Single-Interface and Quantum-Well Heterostructure MISFET's

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Abstract—**The physical operation of heterostructure metal–insulator–semiconductor field-effect transistors (H-MISFET's) is described and compared with that of more familiar heterostructure FET's. Undoped, doped-channel, and quantum-well MISFET's based on AlGaAs/GaAs heterostructures are examined. Focus is placed on quantum-well MISFET's, which differ most from more conventional devices. Results of experiments and simulations are presented to examine the physical mechanisms related to charge-control, gate leakage, device geometry, short-channel effects, buffer leakage, and electron trapping in the devices, and the advantages of other III–V materials systems are discussed. Finally, the potential advantages of H-MISFET's for circuit applications are discussed.**

I. INTRODUCTION

SINCE THE development of the first AlGaAs/GaAs heterostructure field-effect transistors (HFET's) based on modulation doping (MODFET's) [1], many advanced HFET's have been demonstrated. These include MODFET's incorporating pulse doping distributions [2], quantum-well channels [3], alternative material systems [4] including pseudomorphic materials [5], and various combinations of these improved device designs [6]–[10]. In addition, many new types of HFET's have been demonstrated. These devices are similar to the MODFET in that an electron channel is formed in a narrower gap semiconductor layer (e.g., GaAs) while an adjacent wider gap semiconductor (e.g., AlGaAs) serves as a gate barrier. The motivation for the development of these more recent devices has been the elimination of various problems of MODFET's related to threshold uniformity and control, electron trapping instabilities, and limited current drive resulting from parallel conduction and gate-leakage currents.

This paper deals with a class of HFET's which we refer to as heterostructure metal–insulator–semiconductor FET's (H-MISFET's). The "insulator" layer in a H-MISFET is not a true insulator, but rather an undoped semiconductor with a relatively wide band gap such as AlGaAs. In the operation of H-MISFET's, this undoped layer functions as an insulator in that it limits the flow of electrons through the gate in much the same manner as the oxide layer in a silicon MOSFET.

A variety of types of H-MISFET's have been demonstrated. The basic MISFET [11]–[15] consists of a metal gate formed on an undoped two-layer structure, such as AlGaAs/GaAs. The structure shares the advantages of the semiconductor–insulator–semiconductor FET (SISFET) [16]–[18] in that it offers improved threshold control and eliminates electron trapping associated with doping in the AlGaAs layer beneath the gate. The doped-channel MISFET (DC-MISFET) [19]–[22] is similar to the basic MISFET structure, but uses doping in the channel layer to provide increased electron densities. Another type of H-MISFET is the quantum-well MISFET (QW-MISFET) [23]–[26], which is based on a three-layer structure, such as AlGaAs/GaAs/AlGaAs. Quantum-well channel design provides improved electron confinement and, with the incorporation of doping beneath the quantum well, provides increased electron transfer to the channel.

Much of the development of H-MISFET's has been motivated by digital circuit applications. However, these new devices also hold promise for microwave applications. In this paper, we describe results of experiments and simulations aimed at providing a better understanding of these devices and a perspective of their promise for circuit applications. We will deal with those physical aspects of H-MISFET's which differ most significantly from those of the conventional AlGaAs/GaAs MODFET. In doing so, we will focus mostly on the QW-MISFET. This device represents the greatest departure from the conventional MODFET, differing not only in terms of gate leakage, charge control, and trapping effects, but also in the transport in the access regions outside the gate.

II. COMPARISON OF H-MISFET'S WITH OTHER HETEROSTRUCTURE FET'S

Calculated conduction band edges for various AlGaAs/GaAs HFET's at zero gate bias are shown in Fig. 1. The calculations are implemented by a finite-difference, iterative technique to calculate band bending and charge distributions in a heterostructure in one-dimension. Temperature-dependent material parameters and accurate Fermi–Dirac statistics were included together with a com-

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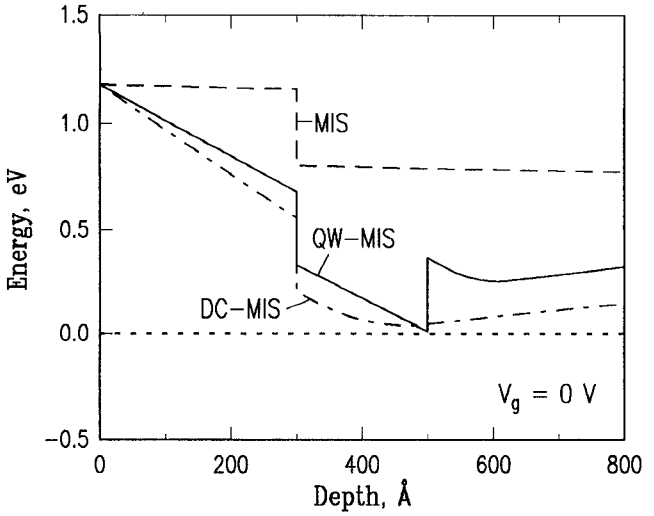

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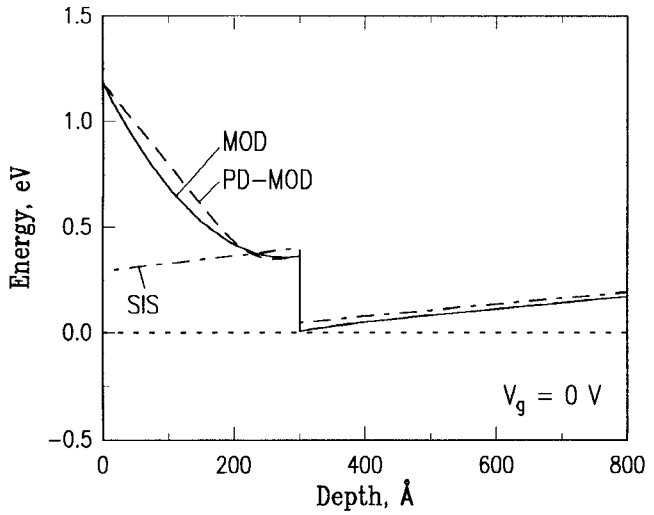


(b)

Fig. 1. Conduction band edge at zero gate bias.

position-dependent deep-donor model that correctly calculates carrier "freeze-out" in the $Al_{0.4}Ga_{0.6}As$ regions.

Fig. 1(a) shows the case for three different H-MISFET's: 1) an undoped MISFET, 2) a quantum-well MISFET with doping beneath the channel (QW-MISFET), and 3) a doped-channel MISFET (DC-MISFET). Fig. 1(b) shows the case for three other HFET's: 4) a conventional modulation-doped FET (MODFET), 5) a pulse-doped MODFET (PD-MODFET), and 6) a semiconductor–insulator–semiconductor FET (SISFET). We will use these acronyms to refer to these devices, since they provide a reasonably consistent set. Other terms commonly used to designate identical or similar devices are, by number, 1) HIGFET, 2) QW MI^3SFET or I^2-HEMT, 3) DMT or H-MESFET, 4) HEMT or SDHT, 5) δ-MODFET, and 6) GaAs-gate FET.

The layers in common in the HFET's of Fig. 1 are the AlGaAs and GaAs layers beneath the gate, which serve to form a potential barrier to gate leakage and serve to define an electron channel in the GaAs layer near the heterointerface. For purposes of comparison, the parameters of similar layers in the different devices in Fig. 1 are identical (see Table I). While these parameters represent a reasonable choice in all cases, optimization of the devices requires some important trade-offs in the parameters, as will be discussed later. In structures having doped layers, the doping concentrations have been chosen to provide a threshold of approximately 0 V. Thus, the zero bias condition in Fig. 1 represents the case of negligible electron accumulation in the channel for all devices, except the MISFET.

TABLE I
HETEROSTRUCTURE LAYER PARAMETERS USED IN SIMULATION

	THICKNESS (nm)/MOLE FRACTION / DOPING (cm^{-3})				
MIS	30/0.4	200/0.0	-	-	-
	-	-	-	-	-
QW-MIS	30/0.4	20/0.0	3/0.4	10/0.4	200/0.4
	-	-	-	$1.5x10^{18}$	-
DC-MIS	30/0.4	20/0.0	200/0.0	-	-
	-	$9.0x10^{17}$	-	-	-
MOD	30/0.4	200/0.0	-	-	-
	$1.5x10^{18}$	-	-	-	-
PD-MOD	17/0.4	10/0.4	3/0.4	200/0.0	-
	-	$3.1x10^{18}$	-	-	-
SIS	100/0.0	30/0.4	200/0.0	-	-
	$2.0x10^{18}$	-	-	-	-

In order to examine the differences between these FET heterostructures, we begin with the familiar MODFET. The MODFET structure consists of a metal gate, a uniformly doped AlGaAs layer, and an undoped GaAs layer. Band bending within the doped AlGaAs layer caused by the presence of ionized impurity centers determines the threshold voltage of the device, which is approximately the difference between the Fermi energy and the lowest point in the conduction band in Fig. 1. (For simplicity, we neglect the effect of quantization in the potential wells.)

The PD-MODFET is similar to the MODFET, except that the doping in the AlGaAs layer is confined to a narrow region near the heterointerface. The restriction of the impurities to a region away from the device surface results in an increased breakdown voltage for the PD-MODFET.

The MISFET heterostructure is identical to that of the MODFET, except that the AlGaAs layer in the MISFET is undoped. This results in a threshold voltage that is fixed by the gate-to-AlGaAs barrier height and the AlGaAs/GaAs conduction band offset. As will be discussed below, the undoped MISFET has advantages over the MODFET

with regard to threshold control, leakage current, and parasitic trapping effects; however, the high threshold voltage of this device is a disadvantage.

The other HFET's in Fig. 1 can be viewed as means of retaining some of the advantages of the MISFET while providing a threshold that is adjustable, or near zero. For example, the SISFET is similar to the MISFET, except that the metallic gate is replaced by a heavily doped semiconductor (N^+ GaAs) in the SISFET. While the threshold is still fixed in the SISFET, the semiconductor gate gives a reduced gate barrier which shifts the threshold to 0 V, as shown in Fig. 1(b). Thus, the drain current and gate current characteristics in the MISFET and SISFET are identical, except for a shift in gate voltage.

In the DC-MISFET, the threshold is adjusted by doping the channel region. Impurities are introduced in approximately 20 nm of the GaAs layer immediately beneath the heterointerface, as shown in Fig. 1(a). Thus, the channel of the DC-MISFET is similar to that of a GaAs MESFET, while the gate potential barrier is similar to that of a MISFET.

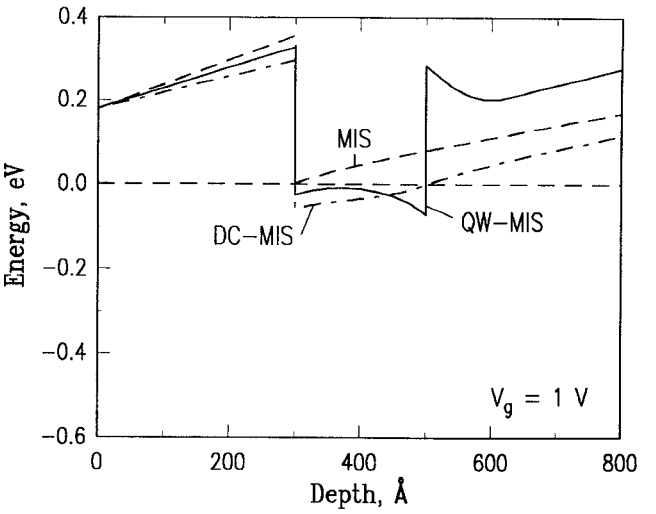
In the QW-MISFET, impurities are incorporated in an AlGaAs layer beneath the channel, as shown in Fig. 1(a). Thus, the heterostructure defines a quantum-well channel sandwiched between an MIS barrier (above) and an inverted interface (below). The impurity layer in the QW MISFET serves the same threshold-shifting (band-bending) function as the impurity layer in the DC-MISFET, without introducing impurity scattering within the channel.

III. Charge Control and Gate Leakage

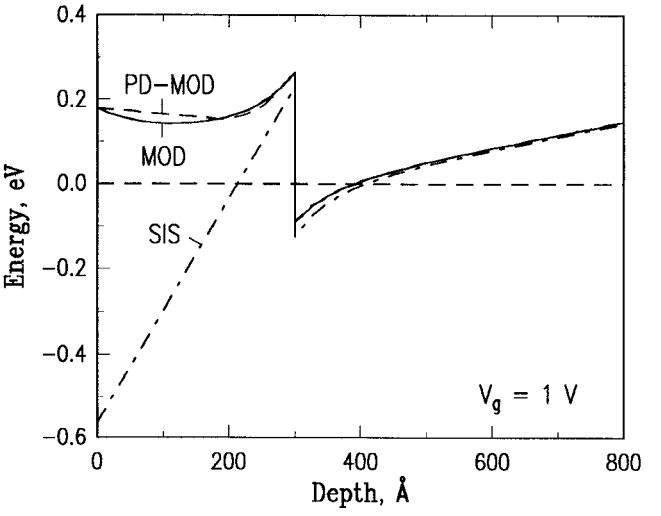
As the gate bias is increased in the forward direction, electrons accumulate in the heterostructures via electron transfer between the layers and through the external circuit. The details of this charge control process are highly dependent on the heterostructure design. The heterostructure design influences not only the electron accumulation in the channel, but also electron trapping within the layers and vertical transport between the layers (gate leakage).

A complete analysis of the forward-biased state is beyond the range of our model since gate current, which affects the quasi-Fermi level position in the AlGaAs layer, has been neglected. However, a basic understanding of the forward-bias state can be obtained under the assumption of constant quasi-Fermi levels within the layers and zero drain bias. In structures where the AlGaAs layer is undoped, we assume that the quasi-Fermi changes abruptly at the heterointerface and is constant elsewhere. This implies essentially zero charge in the AlGaAs layer, which is a good approximation. In structures where the AlGaAs layer is doped, we assume that the impurities are in equilibrium with the channel and, therefore, that the quasi-Fermi level changes abruptly at the gate–AlGaAs interface. This assumption somewhat overestimates the electron density in the AlGaAs layer, but represents a good approximation over a large bias range.

As the gate voltage is increased in the forward direction, gate current flows as a result of thermionic emission over the gate–AlGaAs and AlGaAs/GaAs barriers and of tunneling through these barriers [27], [28]. (At high drain bias, hot-electron injection over the AlGaAs/GaAs barrier also plays an important role [29].) The calculated conduction band edge for the various devices at a 1 V gate bias is shown in Fig. 2. The gate-leakage barriers are quite different for different devices. The thermionic emission barrier is the energy at the heterointerface in Fig. 2, while the effective tunneling barrier is related to the area between the AlGaAs band edge and zero energy in the figure. It can be seen that both the thermionic and tunneling barriers are higher for the three H-MISFET's in Fig. 2(a) than for the three devices in Fig. 2(b). The barriers in the MODFET's, particularly the tunneling barrier, are reduced by the band bending associated with the charge in the doped AlGaAs regions. The low barriers in the SISFET result from the small gate–AlGaAs barrier in this device. Since the thermal and tunneling currents depend exponentially on these barriers, the gate leakage for the MISFET, QW-MISFET, and DC-MISFET should be substantially lower than for the other devices when measured at the same gate bias.



(a)



(b)

Fig. 2. Conduction band edge at 1 V gate bias.

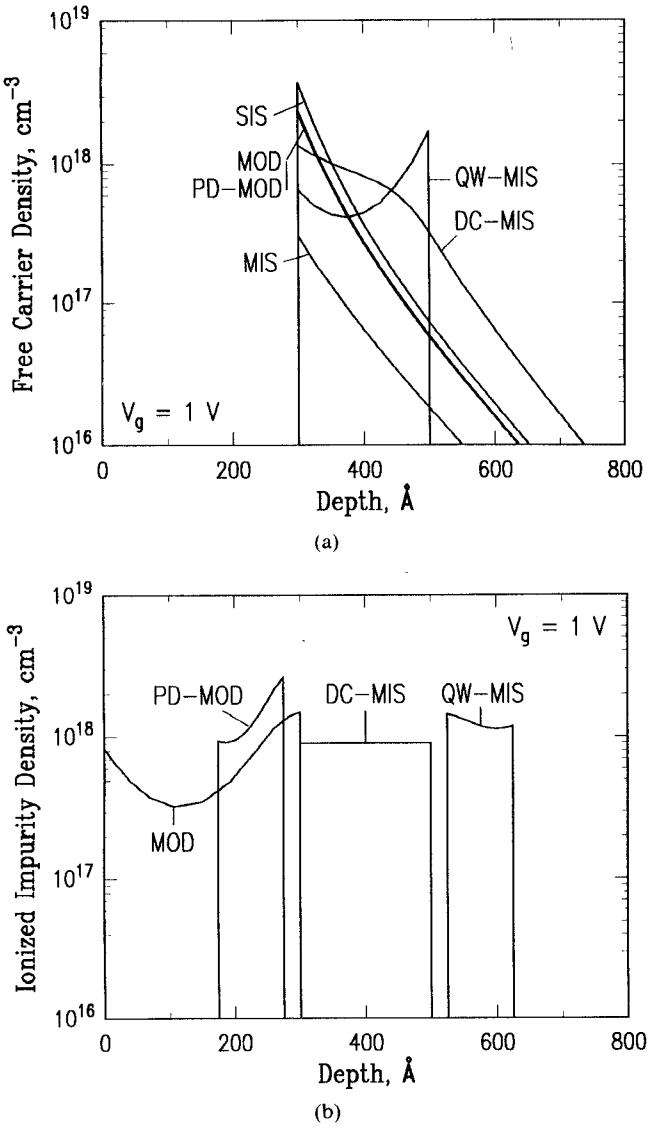


Fig. 3. (a) Free electron density and (b) ionized impurity density at 1 V gate bias.

However, the condition of equal gate bias does not produce equal channel electron densities in the various devices.

The electron accumulation is, in fact, very different for these devices. This is illustrated in Fig. 3, which shows the calculated free electron densities n and the ionized impurity densities N_d^+. The electron distribution is of similar shape for the MODFET's, SISFET, and MISFET, but is different in density. The very low density of the MISFET is simply the result of its high threshold voltage. In order to obtain an electron density equal to that of the SISFET, a bias of 1.8 V would be needed for the MISFET. (The characteristics of these two devices are virtually the same except for a 0.8 V shift.) Thus, although the gate barrier of the MISFET is higher at a given gate voltage, this does not provide an advantage over the SISFET with regard to the maximum channel density for a given gate leakage.

The lower channel density in the MODFET's compared with the SISFET represents a difference in the distribution of electrons between the layers. In the SISFET, all electrons reside in the channel. In the MODFET's, a significant number of electrons enter the AlGaAs layer, where they either are trapped (apparent from the bowing in the N_d^+) or produce parallel conduction in the AlGaAs layer. In either case, these electrons are lost from the high-mobility channel, which is unwanted.

Fig. 3 shows that the electron distributions in the DC-MISFET and QW-MISFET are almost completely confined to the channel, as desired. However, the electron distributions are more spread out in these two devices. This spreading of the electron distribution is a disadvantage since it produces a somewhat lower channel density due to the lower transconductance for electrons farther from the gate.

Gate leakage, parallel conduction, and electron trapping place limits on the maximum channel density $n^{\max}$ for useful operation. The maximum sheet density in MODFET's is limited not only by gate leakage, but also by parallel conduction and trapping. MODFET's with high-mole-fraction AlGaAs layers produce strong trapping instabilities. While low mole fractions minimize these problems, this is at the expense of increased parallel conduction and gate leakage.

As shown in Figs. 2 and 3, the channel densities in the DC-MISFET and QW-MISFET are much greater than in the MISFET at the same gate bias, while the gate-leakage barriers in the three devices are approximately the same. Thus, the DC-MISFET and QW-MISFET offer higher $n^{\max}$ than does the MISFET (or the SISFET, which has the same $n^{\max}$ as the MISFET).

IV. Device Geometries and Source Resistance

H-MISFET's have been fabricated in both recessed-gate (RG) and self-aligned-implant (SAI) geometries, similar to those commonly used for MESFET's and MODFET's. An exception to this is the basic MISFET, which (like the SISFET) requires an SAI geometry because of its fixed positive threshold. The geometries of an RG and an SAI QW-MISFET are shown in Fig. 4.

The influence of the device geometry on current flow in the channel access region outside the gate is particularly important in the case of the QW-MISFET. For high external transconductance, the source resistance components due to the contact resistance R_c and the sheet resistance in the access region r_{sh} must be small. In the RG QW-MISFET, current in the access regions is carried by high-mobility electrons accumulated at the bottom (inverted) interface of the QW channel, as illustrated in Fig. 4. The sheet density n_s of these electrons is comparable to that in a single-interface MODFET, about 1×10^{12} cm^{-2}. The electrons under the gate of the QW-MISFET under high forward bias, on the other hand, may reach a density of more than twice this value, thereby producing the undesirable situation where the sheet resistance in the access region is actually higher than that in the channel.

Channel access in an SAI QW-MISFET is illustrated in Fig. 5, which shows the current flow lines calculated from a conventional drift-diffusion model [26] for a 65 nm $Al_{0.4}Ga_{0.6}As$, 30 nm GaAs, 20 nm $Al_{0.4}Ga_{0.6}As$ (top)

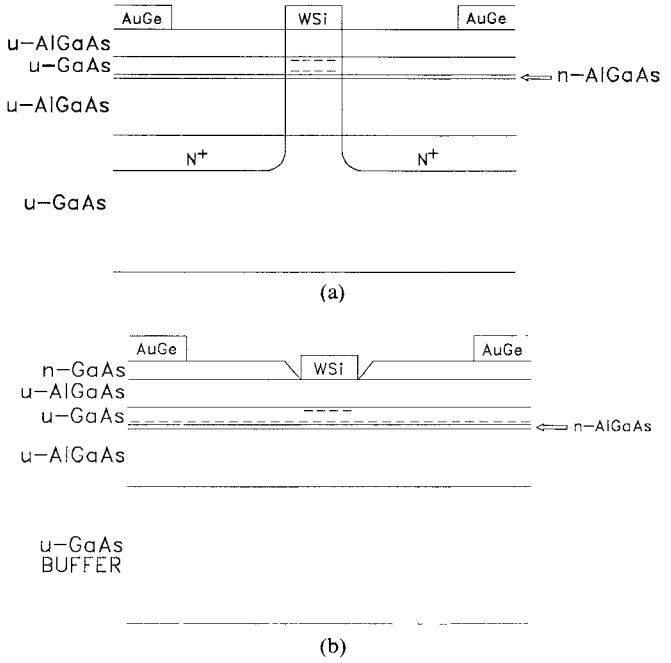


Fig. 4. (a) Self-aligned-implant and (b) recessed-gate QW-MISFET's.

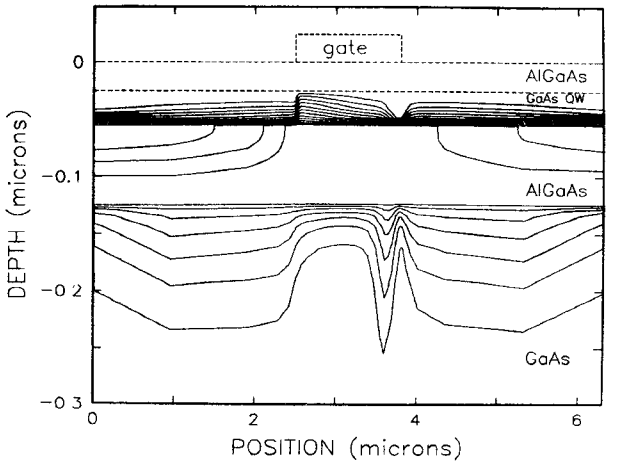


Fig. 5. Current flow lines in a self-aligned-implant QW-MISFET for $V_g = 1$ V and $V_d = 2$ V.

quantum-well structure having a thin doped region 10 nm beneath the well. The Si implant energy and dose used in the calculation are 60 keV and 5×10^{13} cm^{-2}, respectively, and are identical to those used in the experimental devices discussed later. Fig. 5 shows that the current in the AlGaAs layers is very small. This is because of both the deepening of the Si donor level for x greater than 0.2 and the drop in electron mobility as x approaches 0.4, the Γ–X crossover point. Thus, current in the access region of this device must flow primarily through the implanted GaAs layers. A 20 nm GaAs channel doped at 2×10^{18} cm^{-3} provides a sheet density of 4×10^{12} cm^{-2}, which is about four times that for the RG device. However, the increased density in the SAI structure is offset by decreased mobility due to impurity scattering.

The sheet resistance in the access region can be reduced by decreasing the thickness of the bottom barrier layer, thereby increasing the volume of implanted GaAs [26]. However, current flow from the implanted GaAs buffer regions of the quantum-well channel is impeded by the bottom AlGaAs layer when x is high, as seen in Fig. 5, and the FET source resistance is not improved. While some transport across the bottom AlGaAs layer may be possible for very thin, heavily implanted layers, thinning the bottom AlGaAs layer does not appear to be an effective method of reducing the source resistance. In the source resistance experiments below, thick bottom barrier layers are used to minimize conduction in the buffer layer.

TABLE II
DEPENDENCE OF SOURCE RESISTANCE ON HETEROSTRUCTURE DESIGN

Device No.	A	B	C	D	E
h_{TB}, nm	20	20	35	20	20
h_{QW}, nm	25	25	25	40	25
x_{BB}	0.4	0.4	0.4	0.4	0.2
Geometry	SAI	RG	SAI	SAI	SAI
R_c^{300K}, Ω-mm	1.5	0.5	1.9	1.3	0.1
R_c^{77K}, Ω-mm	0.9	0.4	2.2	0.8	0.2
r_{sh}^{300K}, Ω/□	615	850	590	590	380
r_{sh}^{77K}, Ω/□	710	200	650	700	300

The formation of ohmic contacts can also be expected to be influenced by the quantum-well channel. An increase in contact resistance might occur as a result for a higher Al content in the alloyed region for a quantum-well design. In addition, the bottom barrier layer of the quantum well imposes a geometric constraint on the current since current is forced to flow laterally from the contact (in the plane of the channel). This restriction of the current could also increase the contact resistance.

Table II shows the contact resistance and the access region sheet resistance measured in ohmic test sites by the transmission line method for different quantum-well heterostructures. The heterostructure for device A is composed of the following layers: 500 nm GaAs, 120 nm $Al_{0.4}Ga_{0.6}As$, 25 nm GaAs, 20 nm $Al_{0.4}Ga_{0.6}As$, and 5 nm GaAs (top). As grown, the layers are undoped except for a thin doped region 5 nm beneath the quantum well. The SAI test sites are Si implanted (parameters above) and annealed at 875°C by rapid thermal annealing in an arsine atmosphere. The layers for device B, the recessed-gate structure, are identical to that for A, except for the replacement of the 5 nm top layer with a 25 nm n-GaAs layer doped at 2×10^{18} cm^{-3}. No implantation is done in the case of the recessed-gate testers. The heterostructure layers in the other devices are identical to A, except for the variations in top-barrier thickness h_{TB}, quantum-well thickness h_{QW}, or bottom-barrier mole fraction x_{BB} indicated in Table II. The contacts in the test sites are based on a conventional AuGeNi metallization alloyed at 570°C.

Comparison of the RG and SAI devices, B and A in Table II, shows that the SAI device provides some improvement in r_{sh} at room temperature, but exhibits a

higher r_{sh} at 77 K. This is consistent with the discussion of channel electron mobility given above. The R_c of the RG device is substantially lower at both temperatures. This difference cannot be the result of differences in r_{sh} (r_{sh} is higher at one temperature and lower at the other) or cap layer conductivity (GaAs cap depleted in both cases). Hence, these results may indicate a difference in the basic nature of the ohmic contact to the doped channel in the SAI device and to the 2-D electron gas in the RG device.

Devices C and D show little, if any, improvement in r_{sh} compared to A. These heterostructure variations correspond to a shift of the channel closer to the peak of the Si implant profile (86 nm from the surface) and an increase in the channel thickness. If the conductivity in the quantum well were simply related to the as-implanted profile, both devices should provide a substantial reduction of r_{sh}. Hence, it would appear that effects such as compositional disordering, defect propagation, and differences in stopping power between the AlGaAs and GaAs layers favor conductivity near only one interface of the quantum well. The increase in R_c seen for C at 77 K may be the result of the increased Al content in the alloyed region or the greater alloy penetration needed in this case.

Device E is identical to A, except for a reduced mole fraction in the entire bottom-barrier layer. E shows large improvements over the other devices in both R_c and r_{sh}. The increased electron density in the bottom barrier for x equal to 0.2 dramatically increases the conductivity of this layer. In addition, current flow from the implanted region of the GaAs buffer below this layer is possible due to the low interface barrier (which is further reduced by disordering). Note that a low R_c is obtained in this device, despite the high mole fraction (0.4) in the top barrier. This improvement in R_c is probably related to the greatly expanded contact area provided by the conductivity of the lower layers. The source resistance components of device E are as low as those obtained for SAI $Al_{0.3}Ga_{0.7}As$/GaAs MODFET's fabricated by the same SAI process.

While further study is needed to clarify such issues as the electrical activation in implanted quantum wells and the microstructure of the ohmic contacts in quantum-well devices, these experimental results illustrate that access to the channel is more complex in quantum-well heterostructures and that careful optimization of the heterostructure layer parameters is necessary to obtain low source resistance in such devices.

V. Short-Channel Effects and Buffer Leakage Currents

A number of effects contribute to unwanted output conductance g_d in H-MISFET's. Although the electrons in a single-interface heterostructure are confined to a narrow triangular potential well near the source end of the gate (see Fig. 1), the drain potential acts to substantially widen the potential well near the drain end of the gate. The widening of the potential well, together with the heating of electrons in high electric fields, causes electrons to move away from the heterointerface and into the GaAs buffer layer. The channel widening results in an increase in the output conductance [30] in both RG and SAI HFET's.

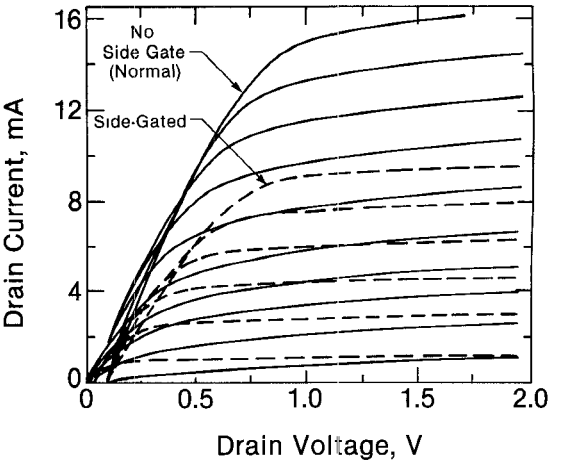


Fig. 6. Current–voltage characteristic at 300 K for QW-MISFET without side-gate bias (solid) and with side-gate bias (dashed).

As the gate length is increased below about 1 μm, g_d increases rapidly as a result of current flow between the closely spaced source and drain regions in the GaAs buffer. Short-channel effects can be severe in SAI HFET's since the tail of the implanted N^+ region may extend thousands of angstroms beneath the interface and the straggle from this implant causes a shortening of the effective channel length. These effects tend to be smaller in RG HFET's where the N^+ regions (the diffused Ge regions within the alloyed contacts) extend only slightly below the channel.

The quantum-well channel design of the QW-MISFET offers a means for eliminating channel-widening effects. In contrast to the case for the triangular barrier in the basic MISFET and other single-interface HFET's, the potential barrier at the bottom of a quantum-well channel is unaltered by the applied drain bias since it is an intrinsic feature of the conduction band. As the drain bias is increased, electrons pushed away from the top interface are confined by the barrier at the bottom interface, thus preventing the channel from widening. This is illustrated in Fig. 5. For a quantum-well heterostructure with a bottom barrier layer (as in Fig. 5), an electron gas forms not only in the QW channel, but also within the triangular potential well formed at the AlGaAs–buffer interface. Channel widening for the electrons at this interface is quite apparent in Fig. 5.

The presence of electrons in both layers allows a direct experiment to be performed to examine the difference between the degree of electron confinement in a quantum-well channel and in the triangular potential formed at a single heterointerface. Fig. 6 shows experimental current–voltage characteristics for an SAI QW-MISFET having the same layer parameters as in Fig. 5. (Examination of the experimental I_d versus V_g characteristic and CV profiling of this device has confirmed [26] the presence of electrons in both layers.) The solid curves in the figure show results for the case where drain current flows partially through this AlGaAs–GaAs interface. In this case,

channel widening is possible and a significant output conductance is observed. The dashed curves show the characteristic when a negative side-gating bias is applied to the sample. The effect of this bias is to raise the conduction band slightly at the AlGaAs/GaAs interface, thus turning off the buffer channel. Comparison of the curves shows a substantial improvement in the output conductance in the side-gated case. SAI MODFET's examined in the same experiment exhibited g_d values comparable in the QW-MISFET's without side-gating and showed no improvement in g_d with a side-gating bias. Hence, we attribute the improvement in g_d in the QW-MISFET to a better confinement for electrons in the quantum-well channel.

A high mole fraction in the bottom barrier is important for obtaining low g_d. In particular, we find g_d to be about four times higher for x_{BB} equal to 0.2 than for 0.4 in the experimental devices of Table II.

Source–drain leakage at the AlGaAs–buffer interface is undesirable not only because of its effect on output conductance, but also because of its influence on the linearity of the drain current versus gate voltage characteristic. It is possible to eliminate the electron gas at the AlGaAs interface by proper heterostructure design. Increasing the thickness of the bottom AlGaAs layers (>1000 Å) serves to eliminate this gas since this raises the energy of the triangular well. Thick bottom AlGaAs layers should also reduce conductivity in the lower AlGaAs layer. An alternative solution is in the incorporation of a p-type impurity layer within the buffer, which acts to raise the energy of the triangular well similar to the situation in a side-gated device. This latter approach, which has been demonstrated for p-channel QW-MISFET's [31], has the advantage of being compatible with thin bottom AlGaAs layers.

Thus, reduced short-channel effects and buffer leakage currents are possible in QW-MISFET's. However, optimization of the bottom-barrier design is necessary to obtain low output conductance together with low source resistance in these devices.

VI. Trapping Instabilities

Instabilities in the electrical characteristics are of potential concern in HFET's having n-type doped AlGaAs layers since n-type impurities produce deep levels in $Al_xGa_{1-x}As$ at x greater than approximately 0.2. The trapping or detrapping of electrons on these centers, which can occur under certain bias or illumination conditions, can cause unwanted threshold shifts and a collapse of the current–voltage characteristic [32]. Due to the large capture and emission barriers for these centers [33], these effects can persist for tens of microseconds at room temperature and indefinitely at cryogenic temperatures.

An increase in the source–drain resistance R_{sd} can occur due to electron trapping in AlGaAs layers. This type of instability is strongly dependent on device geometry. In RG MODFET's, a dramatic increase in source–drain resistance (a collapse in the I_d–V_d characteristic) can occur due to the influence of the trapped-charge dipole on the electron-gas density between the gate and drain [32]. The R_{sd} instability is small in the case of SAI MODFET's [34], apparently because of the low resistance provided by the implanted GaAs region between the gate and drain. Little instability in R_{sd} is also expected for MISFET's, SISFET's, and DC-MISFET's fabricated in similar SAI geometries. Due to the small thickness of the implanted GaAs channel in a QW-MISFET, a somewhat larger source–drain instability might be expected for this device. A recessed-gate DC-MISFET is a particularly attractive device from a trapping point of view, since such devices should be completely free of these effects.

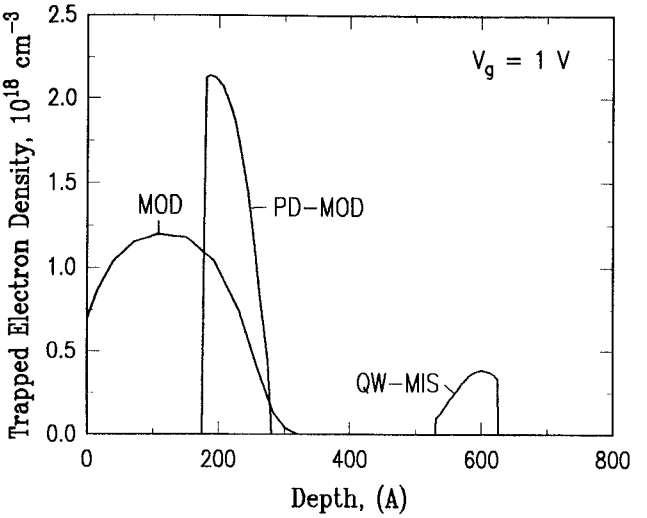


Fig. 7. Comparison of trapped electron distribution in MODFET, PD-MODFET, and QW-MISFET.

A bias-induced shift in threshold occurs in MODFETs as a result of electron trapping in the doped AlGaAs layer beneath the gate. This trapping is strongly dependent on gate bias. As the gate bias is increased beyond threshold, electrons are initially introduced only into the channel, and negligible trapping occurs. As the gate bias is increased further, however, the lowering of the AlGaAs conduction band allows electrons to enter this layer where they may be trapped. Threshold shift is also possible in the PD-MODFET and QW-MISFET, as a result of doping in some fraction of the AlGaAs layers in these devices. Bias-induced threshold shifts should not occur in the MISFET, SISFET, or DC-MISFET since the AlGaAs layers are undoped beneath the gate in these devices.

The details of the electron trapping are different for the MODFET, PD-MODFET, and QW-MISFET. Fig. 7 shows the calculated distribution of trapped charge N_d^0 for the three devices at a gate bias of 1 V. As in the calculation of Figs. 2 and 3, the AlGaAs electrons are assumed to be in equilibrium with those in the channel. The sheet densities corresponding to these distributions are 2.57×10^{12}, 1.59×10^{12}, and 0.29×10^{12} cm^{-2} for the MODFET, PD-MODFET, and QW-MISFET, respectively. The trapped electrons act to change the electric field in the region between the trapping region and the gate. Hence, trapping produces a threshold shift which is dependent on both the density

and the position of the trapped electrons. (Electrons trapped farther from the gate produce larger shifts.)

The threshold shifts determined from the integral of N_d^0 in Fig. 7 are 0.5, 0.5, and 0.2 V for the MODFET, PD-MODFET, and QW-MISFET, respectively. Note that although the trapped electron density is different in the MODFET and PD-MODFET, this does not result in a decreased threshold shift since this difference is offset by the difference in the trapped charge position. The shift is smaller in the QW-MISFET, however, as a result of the screening action of the electrons in the channel. As the gate bias increases beyond threshold in the QW-MISFET, some trapping occurs as the conduction band drops through the Fermi level at the bottom of the well. Once the bottom of the well fills with electrons, however, these electrons screen the doped layer, thereby limiting the trap-filling process.

Although lower than in the other two devices, some threshold shift still occurs in the QW-MISFET. Trapped charge in this device may be thought of as arising from electrons which do not transfer to the gate or to the channel. Hence, trapping in the QW-MISFET can be further reduced by reducing the doping and the width of the impurity layer so as to ensure that the sheet doping density does not exceed the sheet density of electrons that may be transferred to the channel. For the same reasons, positioning the doping as close as possible to the channel (a small spacer layer) is desirable [26].

In order to experimentally examine the trapping instabilities, measurements were made of the bias-induced changes in threshold voltage V_t and source–drain resistance R_{sd} for both QW-MISFET's and MODFET's at 77 K. The devices were fabricated in the same SAI process as described elsewhere [26]. In this experiment, the changes in V_t and R_{sd} are measured in the dark at 77 K before and after one minute of gate and drain bias stress. Measurements for each bias stress are made beginning from illuminated initial conditions (see [32]).

A minimal change in R_{sd} was seen for both the QW-MISFET's and MODFET's. Hence, the smaller volume of implanted GaAs in the QW-MISFET channel does not result in a greater source–drain instability. Significant differences were seen, however, in the stress-induced threshold shift in the two devices. A comparison of the threshold shifts over large ranges of bias stress is given in Fig. 8. For the MODFET, it is seen that the shift increases dramatically for increased gate and drain bias, reaching a level of 0.5 V at the end of the measurement range. In the case of the QW-MISFET, the shift is considerably smaller. For gate and drain biases below 1.5 V, a typical operating range, the threshold shift in the QW-MISFET is less than 0.1 V, despite the high AlGaAs mole fraction (0.4) and thick spacer layer (10 nm) in the experimental structure.

VII. Other III–V Material Systems

We have confirmed our attention mostly to $Al_{0.4}Ga_{0.6}As/GaAs$ H-MISFET's. Due to the Γ-X crossover in $Al_xGa_{1-x}As$ at x equal to 0.4, this mole fraction provides the highest conduction band offset (0.36 eV) and, hence, is close to optimum for obtaining a high heterointerface barrier [28]. The ability to make use of such high mole fractions in H-MISFET's represents a significant advantage of H-MISFET's over MODFET's. Because of trapping instabilities, MODFET's are more typically designed with a mole fraction of 0.3, with the more recent trend being toward values of 0.2 or less [35]. Such low values of x require severe compromises in MODFET design since they result in a small offset (0.18 eV for x equal to 0.2), which increases both gate current and parallel conduction. While AlGaAs layers with nonuniform composition (e.g., PD-MODFET's with low x only in the doped region) can help eliminate instability, parallel conduction in the doped AlGaAs region still limits the forward gate bias in such devices.

In contrast to MODFET's, reductions in band offset and electron density are not required for eliminating instabilities in the MISFET, DC-MISFET, or SISFET. In the QW-MISFET, a low x AlGaAs layer is desirable for the bottom barrier, both for decreasing source resistance and eliminating residual trapping instabilities. However, the value of x in the more critical top barrier layer of this device, as for the other H-MISFET's, is unconstrained.

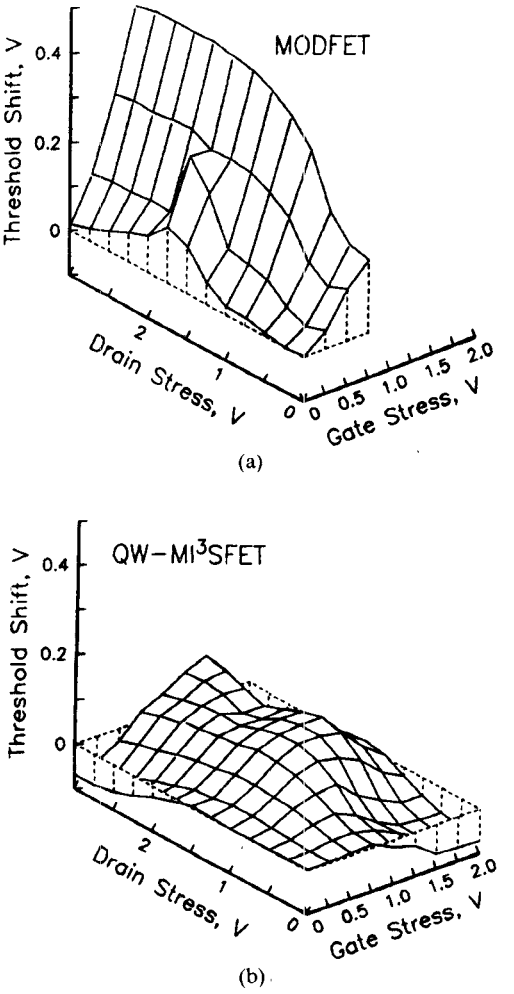


Fig. 8. Comparison of bias-stress-induced trapping in (a) MODFET and (b) QW-MISFET at 77 K.

This means that the advantages of H-MISFET's over MODFET's with regard to barrier height are far greater than indicated by the calculations in Figs. 2 and 8, where equal mole fractions were assumed.

An improvement in the characteristics of all HFET's is possible in heterostructures based on other III–V materials. This is a result of enhanced transport properties [36] and increased band offsets in such heterostructures as $Al_{0.48}In_{0.52}As/Ga_{0.47}In_{0.53}As$ lattice matched to InP. The larger conduction band offset (0.52 eV) and the reduced trapping effects [37] in this material system ease the trade-off between barrier height and instability for MODFET's. However, the lower metal–$Al_{0.48}In_{0.52}As$ barrier height (0.67 eV compared to 1.17 eV for $Al_{0.3}Ga_{0.7}As$) leads to increased gate leakage and parallel conduction. Thus, $Al_{0.48}In_{0.52}As/Ga_{0.47}In_{0.53}As$ H-MISFET's [15], [25] should retain their advantages over MODFET's in this material system with regard to improved channel densities.

Pseudomorphic (strained) channels have been employed in a variety of HFET's [5], [7], [10]. For example, the low band gap of InGaAs has been exploited with much success in $Al_xGa_{1-x}As/In_yGa_{1-y}As/GaAs$ MODFET's, where the $In_yGa_{1-y}As$ channel in this structure results in an increased conduction band offset compared to GaAs. In order to avoid trapping instabilities in MODFET's, however, some compromise must be made in exploiting this increased offset. In order to avoid trapping, x must be less than 0.2 in the $Al_xGa_{1-x}As$ layer. The value of y in the $In_yGa_{1-y}As$ layer is limited by lattice strain to about 0.15. Thus, the band offset in this case is no greater than that for an $Al_{0.3}Ga_{0.7}As/GaAs$ MODFET. In pseudomorphic MISFET's, SISFET's, and DC-MISFET's [20], [21], on the other hand, such a compromise is not necessary, and offsets as high as 0.46 eV should be attainable in $Al_{0.4}Ga_{0.6}As/In_{0.15}Ga_{0.85}As$ H-MISFET structures.

Pseudomorphic InGaAs channels obviously involve some form of quantum-well band structure and, hence, may be most fully exploited in QW-MISFET designs. The use of pseudomorphic layers in a QW-MISFET provides an attractive means for satisfying the trade-offs in layer parameters discussed in the previous sections. Specifically, the combination of the high-x top barrier, InGaAs channel, and low-x bottom barrier in an $Al_{0.4}Ga_{0.6}As/In_{0.15}Ga_{0.85}As/Al_{0.2}Ga_{0.8}As$ QW-MISFET is suitable for achieving low gate leakage and high electron density, together with low parasitic resistance and instability-free operation.

VIII. Circuit Applications

In this section we examine how the details of H-MISFET designs impact the potential digital or analog circuit applications for these devices. The speed of enhance/deplete (E/D) digital circuits is strongly dependent on the current-drive capability of enhancement-mode (normally-off) FET's. E/D logic, which is analogous to silicon NMOS logic, has been used extensively in GaAs MESFET and MODFET circuitry. The need to operate under forward gate bias leads to limitations in HFET circuits related to potential instability and the much higher gate leakage in HFET's compared to silicon MOSFET's. These effects limit the useful swing of gate voltage, making noise margin requirements more severe.

The fixed positive threshold, the absence of trapping instabilities, and the large barrier in MISFET's address some of the limitations of MESFET's and MODFET's in E/D circuits. A drawback of the MISFET, however, is its high threshold voltage (0.8 V). The higher threshold results in a lower drain current for a given gate bias, thereby offsetting some of the MISFET's advantages.

The drawback of the high threshold in the MISFET is overcome in the SISFET, which has a threshold near zero and electrical characteristics virtually identical to those of the MISFET (when measured with respect to threshold). Hence, when operated at the maximum supply voltages for comparable gate-leakage limits, SISFET's should provide a higher large-signal transconductance (ratio of drain current to gate voltage) and lower propagation delays than MISFET's. On the other hand, the higher threshold of the MISFET provides an advantage over the SISFET for complementary circuits, where low static drain currents are required.

The QW-MISFET is attractive for E/D logic since it offers the high barrier of the MISFET together with the low threshold of the SISFET and, hence, potentially offers the highest leakage-limited large-signal transconductance. Although the doping beneath the quantum well means that threshold control is more difficult for this device, the ability to optimize the threshold voltage is an important advantage in circuit design. The high gate barrier and adjustable threshold of the QW-MISFET are particularly attractive for complementary circuits [31] with low static gate and drain currents. In addition, the possibility of enhanced hole transport properties [10] in pseudomorphic QW-MISFET designs makes this device particularly attractive for complementary circuit applications.

The DC-MISFET possesses many of the advantages of the QW-MISFET. However, the DC-MISFET suffers from degraded transport properties caused by the presence of impurities in the channel. The lower channel mobility near threshold results in a lower K factor ($K = \partial g_m / 2 \partial V_g$), which means that the drain current increases more slowly above threshold. This represents a drawback in enhancement-mode FET's where the gate voltage swing is limited.

The FET requirements for microwave amplifier applications are somewhat different from those for digital circuits. For example, threshold voltage control is not as critical a parameter in microwave FET's, whereas the requirements on linearity can be much more severe for these applications.

The advantages of H-MISFET's with regard to gate leakage, channel density, and trapping instabilities can be exploited in microwave power FET's. Not only can the range of positive gate voltage be increased by the higher leakage barrier in H-MISFET's, but the range of negative voltage can also be increased. This is because the undoped

condition of the barrier layer in H-MISFET's should result in an increased source–drain breakdown voltage. Although it is not possible to take advantage of this negative range in the undoped MISFET due to its fixed positive threshold, the DC-MISFET is attractive for exploiting this potential increase in RF amplitude. The lower K factor expected in DC-MISFET's is not of much concern for such applications since the voltage range is relatively large. Similarly, depletion-mode QW-MISFET's may also offer advantages for extending the RF swing. However, the values of negative threshold are more limited in this device because of limitations on doping sheet density mentioned above.

The linearity of the I_d versus V_g characteristic is critical in microwave applications requiring amplitude or phase linearity. In this case it is essential to eliminate parallel conduction and to minimize the variation in the gate-to-charge distance with gate voltage. The triangular potential well in the MODFET reduces the variation in gate-to-charge distance compared with that in MESFET's. However, the linear range of gate voltage is fairly small in MODFET's as a result of the limited channel densities. The linear range should be somewhat larger for the undoped MISFET and SISFET. While DC-MISFET's and QW-MISFET's offer larger operating ranges, good linearity in these devices would require small channel thicknesses.

Cutoff frequency and gain are, of course, prime figures of merit for microwave amplifiers. Electron mobility and channel density are key parameters affecting cutoff frequency in low-noise amplifiers [6], [38], where operation near pinch-off is essential. A potential advantage of the MISFET's and SISFET's is related to the absence of scattering by impurity centers in these structures (an effectively infinite spacer thickness), which results in high low-temperature mobilities. The low mobility in the DC-MISFET channel represents a disadvantage for low-noise applications with this device. Due to its low output conductance, the QW-MISFET is particularly promising for high-gain amplifiers. In addition. The possibility of reduced short-channel and buffer-leakage effects in QW-MISFET's is attractive for scaling to very short channel lengths, particularly in the case of SAI devices, which have been more limited in this respect.

An additional consideration is the possibility for improved noise performance due to the reduced scattering for electron systems of lower dimensionality (e.g., a two-dimensional electron gas). The improved confinement in the QW-MISFET may be particularly attractive from this point of view.

IX. Concluding Remarks

We have attempted to provide a basic understanding of the physical operation of H-MISFET's and their promise not only for digital, but also for microwave circuit applications. In order to illustrate the important features of H-MISFET's, comparisons have been made between these devices and a conventional MODFET. It should be emphasized that some overlap exists between the wide variety of advanced MODFET's demonstrated to date and the H-MISFET's considered here. In particular, the quantum-well channel design emphasized in this paper has also been highly exploited in MODFET designs. Hence, some of the issues raised in this paper, such as transport in confined access regions, relate to other HFET's as well.

This study has been restricted to some of the more fundamental aspects of H-MISFET operation. Determining the overall potential of a device for a specific application is complicated by the need to assess a wide range of trade-offs in device design and circuit performance. This involves not only heterostructure design, but also the consideration of the relevant materials growth and fabrication issues. Such technological considerations have had an important impact on the HFET designs in dominance today. However, their ultimate impact is more difficult to assess due to the rapid advancement in III–V growth and fabrications technologies over time.

It is hoped that this paper will help indicate some general directions for further improving heterostructure FET's, particularly for microwave applications.

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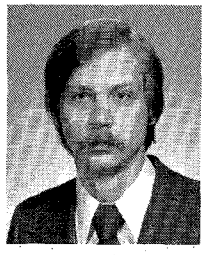

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